IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Kevin Kwong-Tai CHUNG

Application No.: Not Yet Assigned

Attorney Docket No.: AI-TECH-16B

Filed: Herewith

For: FLEXIBLE DIELECTRIC
ELECTRONIC SUBSTRATE AND
METHOD FOR MAKING SAME

Examiner:

Group Art Unit:

CERTIFICATE OF MAILING UNDER 37 C.F.R § 1.8(a)

I hereby certify that this Correspondence is being deposited on the date identified below with the United States Postal Service as first-class mail in an envelope properly addressed to COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450.

February 9, 2004
Date of Certificate

Jacqueline D. Bailey

Commissioner for Patents
Alexandria, VA 22313

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97

In compliance with the duty of disclosure set forth in 37 C.F.R. § 1.56, Applicants are submitting herewith a Form PTO-1449. This Information Disclosure Statement is being filed with a newly filed application. Accordingly no fee is required.

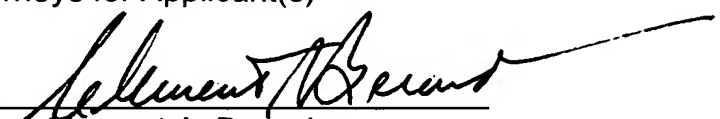
Pursuant to 37 C.F.R. §1.98(d), the captioned Application is a continuation of earlier filed U.S. Application No. 09/578,583 filed by Kevin Kwong-Tai Chung on May 25, 2000 entitled "HIGH-DENSITY ELECTRONIC PACKAGE, AND METHOD FOR

MAKING SAME" (AI-TECH-16A), which is relied upon for an earlier effective filing date under 35 U.S.C. §120, and in which the same items cited in the accompanying form PTO-1449 were cited in one or more Information Disclosure Statements compliant with paragraphs (a) and (c) of 37 C.F.R. §1.98,or are US patents and/or US patent publications that were cited by the Examiner therein.

Applicants respectfully request full and proper consideration of the listed information during examination of the application, and that the listed information be printed on any patent that issues therefrom.

Respectfully submitted,

DANN, DORFMAN, HERRELL & SKILLMAN
A Professional Corporation
Attorneys for Applicant(s)

By 
Clement A. Berard
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Enclosures - Form PTO-1449
Copies of references listed on PTO - 1449

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First Named Inventor: Kevin Kwong-Tai Chung
Group Art Unit: Not Yet Assigned
Examiner Name: Not Yet Assigned
Attorney Docket Number: AI-TECH-16B

SHEET 1 OF 3

UNITED STATES PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	PATENT NUMBER	ISSUE DATE MM-DD-YYYY	FIRST NAMED INVENTOR
		5,950,304	09/14/1999	Khandros, et al
		5,915,170	06/22/1999	Raab, et al
		5,848,467	12/15/1998	Khandros, et al
		5,685,885	11/11/1997	Khandros, et al
		5,682,061	10/28/1997	Khandros, et al
		5,929,517	07/27/1999	DiStefano, et al
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		5,367764	11/29/1994	DiStefano, et al
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		5,148,265	09/15/1992	Khandros, et al
		5,777,379	07/07/1998	Karavakis, et al

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	DOCUMENT NUMBER	COUNTRY OR REGION	DATE OF PUBLICATION MM-DD-YYYY	FIRST NAMED INVENTOR OR APPLICANT
		WO 98/26476	PCT	18/06/1998	DiStefano, et al
		WO 98/44564	PCT	08/10/1998	DiStefano, et al

OTHER PRIOR ART - NON-PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in Capital Letters), title of the article (when appropriate), title of the item(book, magazine, journal, serial, ~~symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published~~
		CO VAN VEEN, IC Packaging And Assembly Issues For Next Generation Miniaturised Consumer Electrons, Future Fab International,, Pages 379-382 (4 Pages).
		JACK FISHER, Advancements in Multilayer Material Technology, Future Circuits International, 4 Pages

EXAMINER'S SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw a line through citation if citation not in conformance and reference not considered. Include a copy of this form with next communication to applicant.

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Attorney Docket Number: AI-TECH-16B

SHEET 2 OF 3

UNITED STATES PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	PATENT NUMBER	ISSUE DATE MM-DD-YYYY	FIRST NAMED INVENTOR
		5,371,654	12/06/1994	Beaman et al.
		3,555,364	01/12/1971	Matcovich
		5,798,564	08/25/1998	Eng et al.
		5,043,794	08/27/1991	Tai et al.
		4,734,825	03/29/1988	Peterson
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		5,943,213	08/24/1999	Sasov
		5,394,303	02/28/1995	Yamaji
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OTHER PRIOR ART - NON-PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in Capital Letters), title of the article (when appropriate), title of the item(book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		PETRI SAVOLAINEN, Area Array Packages And High-Density Printed Wiring Boards, Future Circuits International, Pages 193-195 (3 Pages).
		PATRICK THOMPSON, Chip-scale Packaging, IEEE Spectrum, August 1997, Pages 36-43 (8 Pages).
		DENNIS HERRELL, Power to the Package, IEEE Spectrum, July 1999, Pages 46-53 (8 Pages).
		VERN SOLBERG, Chip-Scale Array Devices, Future Circuits International, 5-Pages.
		JOAN TOURNÉ, The Future Of Non-Woven Laminates, Future Circuits International, Pages 129-131 (3 Pages).
		WALTER OLBRICH, High Density Printed Circuit Board Technologies, Future Circuits International, Pages 133-138 (6 Pages).
		IVAN HO, Microvia Technology, Future Circuits International, Pages 139-141 (3 Pages).

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SHEET 3 OF 3	Attorney Docket Number: AI-TECH-16B

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		5,192,716	03/09/1993	Jacobs
		5,794,330	08/18/1998	DiStefano, et al
		5,901,041	05/04/1999	Davies et al
		5,783,870	07/21/1998	Mostafazadeh et al
		5,672,548	09/30/1997	Culnane et al
		5,686,699	11/11/1997	Chu et al
		5,172,303	12/15/1992	Bernardoni et al
		5,286,926	02/15/1994	Kimura et al

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		DIETER BERGMAN, BGAs The Component Package Of Choice, Future Circuits International, 7 Pages.
		MARK HUTTON, High Density Substrates for IC Packaging, Future Circuits International, 3 Pages.
		RAVI M. BHATKAL, Techno-Economic Analysis of Alternative Wafer Bumping Technologies, Future Circuits International, 4 Pages.
		International Search Report, PCT/US00/13077, 18 August 2000 (2 Pages)

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